Master Thesis

„FPGA implementation of a DAQ and Control System for a miniaturized Fourier Transform Spectrometer "

About us

CTR Carinthian Tech Research AG is an industry-oriented research and development center for „Smart Sensors and Systems Integration". As the largest non-university research center in southern Austria, CTR has gained a reputation for expertise in R&D sensor technologies serving science and industry at both national and international level. CTR focuses on four main research areas: Microsystem Technologies, Heterogeneous Integration Technologies, Photonic Sensor Systems and Smart Systems. CTR is part of Austria's COMET research program with the K1 excellence center "ASSIC Austrian Smart Systems Integration Research Center".

Short description

Together with an industry partner, CTR currently develops a compact, rapid scan, near-infrared Fourier transform spectrometer. The central control unit is micro module from Trenz Electronic integrating a Xilinx Spartan-6 LX FPGA. For proper operation the device requires control of two quasi resonant micro-mechanical scan mirrors, a data-acquisition system synchronized to the response of an optical reference interferometer, performance of a FFT and an appropriate memory and communication management for data averaging and output. While some of the basic functionalities are already implemented, important parts still remain to be added or improved.

Tasks

Within the framework of the overall control and data acquisition system, the student will implement and test additional data processing and control routines on the mentioned FPGA board. In particular these are:

(i) Implementation of a FFT in accordance with the synchronized DAQ scheme and the related memory and data-communication management.
(ii) Phase-locking of the micro mechanical mirrors based on signals derived from an optical reference interferometer.

Further the student will perform intense tests on the fully integrated device.

Start Date / Duration / Contract

Start date (planned): 01.02.2018, or as mutually agreed
Contract: We offer you a salaried position including all related rights and duties for employer and employee. The position will be time limited according to the duration of the master thesis.
Duration (planned): 6 months
Place: Villach

Profile / requirements:

- Student in one of the following fields: Electrical engineering, electronics, or related (FH or TU)
- Experience: Excellent knowledge in VHDL programming and softcore-implementation (Xilinx ISE, EDK and SDK), Knowledge and experience of the Xilinx Spartan 6 family
- Basic knowledge in analog and digital electronics, C/C++ programming

Application: www.ctr.at/en/application or www.ctr.at/bewerbung

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